REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. Claims 6, 9, 16, 19 and 20 were previously cancelled. Existing claims 1-5, 7, 8-15, 17, 18 and 21-24 (as previously amended) remain in the application.

ARGUMENT

Claim Rejections – 35 U.S.C. § 103

Claims 1-4, 10-14, and 21-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent 6,185,692 granted to Wolford (hereinafter Wolford) in view of US Patent 5,625,826 granted to Atkinson (hereinafter Atkinson).

Claim 1, as currently amended, is as follows (emphases added),

> "a variable speed bus, *the variable speed bus initialized with a first clock frequency*;
>
> a first unit coupled to the variable speed bus, *the first unit having a first rate of requests to access the variable speed bus*;
>
> a second unit coupled to the variable speed bus, *the second unit having a second rate of requests to access the variable speed bus*; and
>
> an arbitration and bus clock control unit to *monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate*."

Wolford does not teach or suggest at least at least the above emphasized portions of currently amended claim 1. Wolford does describe a data processing

system including a bus, one or more loads coupled to the bus, and a clock generator, and the clock generator dynamically sets the clock frequency for the bus in response to the number of loads coupled to the bus (see Abstract; Fig. 1; col. 3, lines 6-19, 37-42; col. 4, lines 6-12, 34-41 and 62-66 of Wolford). However, Wolford only describes change the bus clock frequency based on the number of loads coupled to the bus whether the loads are active or idle. Wolford does not describe an arbitration and bus clock control unit that monitors the rates of requests to access the bus from various loads and determines a new clock frequency for the bus *based on the rates of requests to access the bus*.

In response to Applicant's above arguments in the final Office Action dated May 21, 2007, the Examiner admitted that Wolford does not expressly show change of clock frequency based on access request rate. However, the Examiner asserted that this feature was well know in the data processing art at the time the invention was made as evidenced by Atkinson by citing col. 8, lines 9-13 of Atkinson. Applicant respectfully disagrees. The cited portion of Atkinson states, "said processor including a frequency adjuster coupled to said count latch and said clock, said frequency adjuster for adjusting the operating frequency of the processor clocking signal based on the counted memory access request." In marked contrast, claim 1 (as amended) recites "*an arbitration and bus clock control unit* to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate." The recited limitation is about an arbitration and bus clock control unit which determines *the clock frequency for the variable speed bus*

based on the bus access rate. The recited limitation is not to change the clock frequency of a *processor* based on the *memory access rate*, as disclosed in Atkinson. Atkinson does not disclose changing only the clock frequency of a variable speed bus.

The Examiner also asserted that the claimed limitation is straightforward possibility in the art and does not require the exercise of inventive skill. Applicant also disagrees. Changing of a processor's clock frequency is known for a while as showing by different power saving states. For example, when there is no activity including memory access activity, the processor may be put in "hibernation" or "standby" state, which basically changes the clock frequency of the processor. For so many years when the technology for changing a processor's clock frequency is known, no one (at least none has been found yet) has ever come up with a technology for changing the clock frequency of a bus until the disclosed application. Indeed, the present application discloses a technology that solves a long-felt problem and is more effective than changing the clock frequency of the entire processor to conserve power consumption of a computer. Thus, the claimed limitation is not obvious over Wolford in view of Atkinson. Applicant respectfully requests that the 35 U.S.C. 103 rejections of claim 1 be withdrawn.

Independent claim 10 includes similar limitations to those emphasized for claim 1 above. Based on the arguments presented above for claim 1, claim 10 is not obvious over Wolford in view of Atkinson. Because independent claims 1 and 10 (as amended) are now patentable over Wolford in view of Atkinson, all of the claims that depend therefrom (i.e., claims 2-5, 7, 8, 21-23 and claims 11-14, 15, 17, 18, 24; respectively) are also patentable over Wolford in view of Barr. Accordingly, Applicant respectfully

requests that the 35 U.S.C. § 103(a) rejections of claims 1-4, 10-14, and 21-24 over the combination of Wolford and Barr be withdrawn.

Claims 22-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wolford in view of Atkinson, and further in view of Barr.

As mentioned above, the combination of Wolford and Atkinson does not teach or suggest all of the limitations recited in currently amended independent claims 1 and 10. Barr was not cited to cure those deficiencies in Wolford or Atkinson. Because claims 22-23 depend from independent claim 1 and claim 24 depends from independent claim 10 and because independent claims 1 and 10, as currently amended, are patentable over Wolford in view of Atkinson, and further in view of Barr, claims 22-24 are thus patentable over Wolford in view of Atkinson, and further in view of Barr. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejections over Wolford in view of Atkinson and further in view of Barr of these claims be withdrawn.

Claims 5, 7, 8, 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolford in view of Atkinson, and further in view of common knowledge in the data processing art at the time of the invention.

As mentioned above, the combination of Wolford and Barr does not teach or suggest all of the limitations recited in currently amended independent claims 1 and 10. The common knowledge in the data processing art was not cited to cure those deficiencies in Wolford or Atkinson. Because claims 5, 7, 8 depends from independent claim 1 and claims 15, 17, and 18 depends from independent claim 10 and because

independent claims 1 and 10, as currently amended, are patentable over Wolford in view of Atkinson, and further in view of common knowledge in the data processing art, claims 5, 7, 8, 15, 17 and 18 are thus patentable over Wolford in view of Atkinson, and further in view of common knowledge in the data processing art. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejections over Wolford in view of Atkinson and further in view of common knowledge in the data processing art of these claims be withdrawn.

CONCLUSION

Based on the foregoing, it is submitted that that all active claims are presently in condition for allowance, and their passage to issuance is respectfully solicited. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Entry of this amendment is respectfully requested.

Respectfully submitted,

Date: September 21, 2007

/Guojun Zhou/
Guojun Zhou
Registration No. 56,478
INTEL CORPORATION
MS JF3-147
2111 NE 25th Ave.
Hillsboro, OR. 97124